Pearl
Semiconductor

SpurFree™

Patented All-Digital Ultra-Low Noise PLL Architecture
- Enabled by a novel DSP engine
- Continuous removal of fractional spurs

Wide Range of Output Frequencies
- 0.2 to 3000 MHz

State-of-the-art Noise Performance
- Typical 90 fs integrated RMS phase jitter spur-inclusive
- Noise performance is maintained across output frequencies

Ideal Timing IC Technology for Next Generation Datacenters Connectivity Applications

Foundation Technology for a Family of Timing IC's
- Programmable Reference Clocks (XO, VCXO)
- Clock Generators & Clock Buffers

Ultra-Low Noise PLL Architecture

SpurFree™

Ultra-Low Noise PLL Architecture

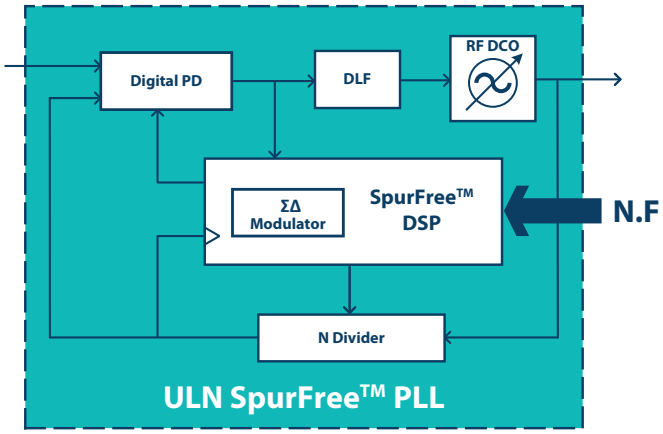
Core Technology

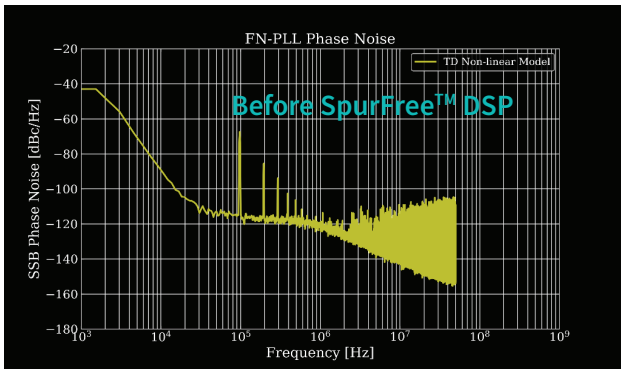
To address the growing demand for new timing solutions achieving better noise performance than currently available state-of-the-art , Pearl Semiconductor developed SpurFree™ PLL architecture.

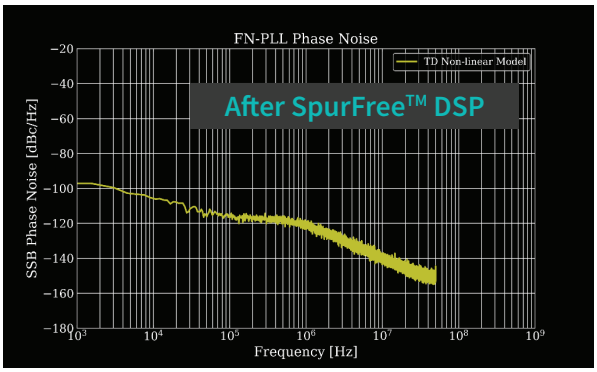
SpurFree™ is a patented All-Digital Ultra-Low Noise PLL architecture enabled by a complex DSP engine. SpurFree's DSP engine substantially attenuates "fractional" spurs induced by the traditional sigma-delta fractional-N loop within the PLL.

Design Novelties:

1. High Precision All-Digital Phase Detector
2. Multiple Feedback Loops to eliminate any Fractional Phase Error
3. RF Wide Tuning Range Digitally Controlled Oscillator
4. Sigma-Delta Modulator allowing Frequency Steps as low as 2 ppb







Family of Products

Pearl is developing a complete full-breadth of timing products based on the SpurFree technology to serve all verticals of the datacenters connectivity market.
Next-Generation datacenters connectivity standards require Ultra-Low Noise Timing Solutions.

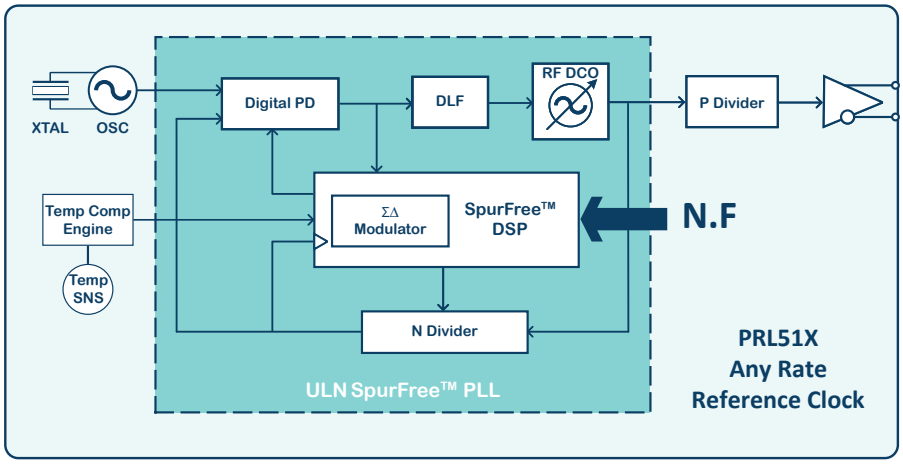
Reference Clocks	PRL51X	• XO/VCXO • Prog. O/P Freq • Ultra-Low Noise
Reference Clocks	PRL501	• XO/VCXO • Ultra-Low Noise • Optical Pluggables
Clock Generator	PRL451X	• Multi O/P • Ultra-Low Noise
Jitter Attenuator	PRL651X	• Multi O/P • Prog. PLL BW • Ultra-Low Noise

SpurFree™ Enabled

Pearl Semiconductor

PRL51X

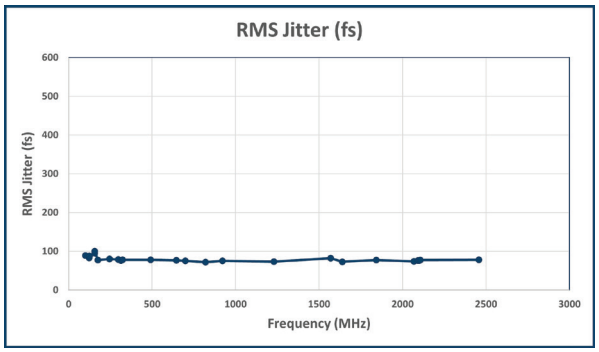
PRL51X is the World's Lowest-Jitter Programmable XO/VCXO Family.



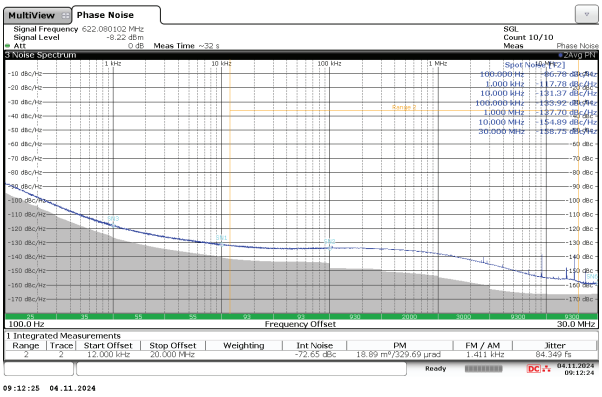
Key Features:

- XO, VCXO & DCXO modes
  - 6-pin and 8-pin packages
- Single, Dual, Quad and I2C Options
- Any-Rate Programmable Frequency
  - 0.2 to 3000 MHz
  - CMOS upto 250MHz
- Ultra-Low Jitter
  - 90 fs Typ RMS - (12kHz – 20 MHz)
- Supply Voltages: 3.3, 2.5 & 1.8V
- Different O/P Formats
  - CMOS, Dual o/p in-phase and complementary
  - LVDS, CML, HCSL, LVPECL, HCSL Fast
- Temp Compensation mode
  - ±3 ppm -40 – 85 °C
- Package Sizes
  - 5032
  - 3225

Outstanding Performance



RMS Jitter for Different Frequencies up to 3GHz



Phase Noise Plot for O/P Frequency = 622.08MHz

LVDS O/P - RMS Jitter = 84 fs

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