

SingleDieTM



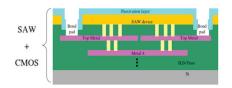
Single-Die Reference Clock Technology

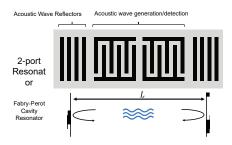
SingleDie[™]

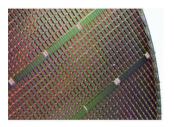
Single-Die Reference Clock Technology

Core Technology

- A fully Single-Die technology where the MEMS SAW Resonator is implemented using a few extra mask layers on top of the CMOS die
 - Eliminates the need for a XTAL or a separate MEMS die
- Pearl uses Silterra's Automotive certified (IATF16949-2016) CMOS technology
- Zero Thermal Latency for excellent temperature compensation
- Extended Operating Temperature Range up to +125 °C
- High Shock & Vibration Resistance
- Suitable for Automotive and Industrial Applications
- Pearl developed a Silicon-Cap on top of the SingleDie™ wafer to include it in an all plastic package





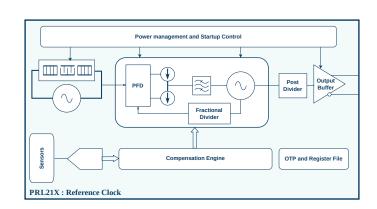


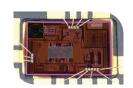
PRL21X Family

Using SingleDie[™] Technology, Pearl developed a superior product family, **PRL21X**. PRL21X features a MEMS SAW resonator on top of a superior CMOS PLL to build the foundation silicon for a complete family of reference clock products.

Key Features

- XO & VCXO
- Single, Dual, Quad or Any-Rate Frequency Options
- Output Frequency Range
 - 1 1000 MHz
- Low Jitter
 - 350 fs Typ RMS (12kHz 20MHz)
- Industrial Operating Temperature
 - -40 +125 °C
- 30 ppm Total Stability option
 - 15 ppm across temperature -40 +125 °C
- LVPECL, LVDS, CML, HCSL and Dual CMOS output options
- 3225 Plastic Package & 5032 Ceramic Package



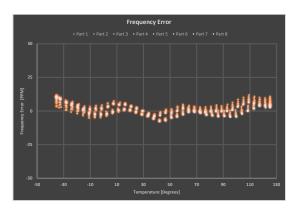


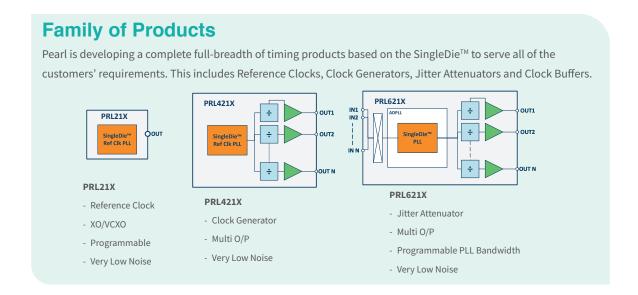




PRL21X Superior Performance

- Achieves a superior stability across temperature
 - 15 ppm from -40 to +125 °C
- Utilizes a novel temperature compensation engine
 - Zero Thermal Latency between MEMS & CMOS die
- Enviornmentally compensated
- Ideal candidate for industrial and automotive applications





Chiplet Option

SingleDie™ technology products can be offer in optional Chiplet die form with bumps that may be flip-chip soldered alongside other chiplets and devices on a substrate in a System in Package (SiP). This is a unique first in the market offering of a programmable Reference Clock chiplet and Clock Generator integrated inside the SiP. Typically may be used in AI modules with demanding timing solutions for data computation and communication with many benefits:

- Efficient placement of the Reference Clock(s) resulting in shorter routing and higher frequency clocks and data rates.
- Saving two pins on the SiP package compared to an externally connected packaged reference clock on the board.
- Higher security level as the system clock is not accessible to be glitched or hacked disturbing any data processing or communication.
- Programmability of the clock(s) during operation allowing different modes of operation and saving power.



www.pearlsemi.com

3 Khalid Ibn AlWaleed St., Sheraton Heliopolis, Cairo, Egypt.

Tel: +202 - 22 69 00 75 **Email:** info@pearlsemi.com