

PR21X

SingleDie™ MEMS-Based Low Noise XO/VCXO Family

Key Features

XO, VCXO & DCXO Modes

Family of Products

- Single
- Dual
- Quad
- Any-Rate (I2C)

Any-Rate Programmable Frequency

- 1 to 1000 MHz

Very-Low Jitter

- Sub-350 fs Typ RMS (12kHz - 20MHz)

Different Packages

- Plastic
- Ceramic
- Chiplet

Extended Operating Temperature

- -40 - +125 °C

Tight Temperature Stability Option

- ±15 ppm (-40 - +125 °C)

Different Supply Voltages

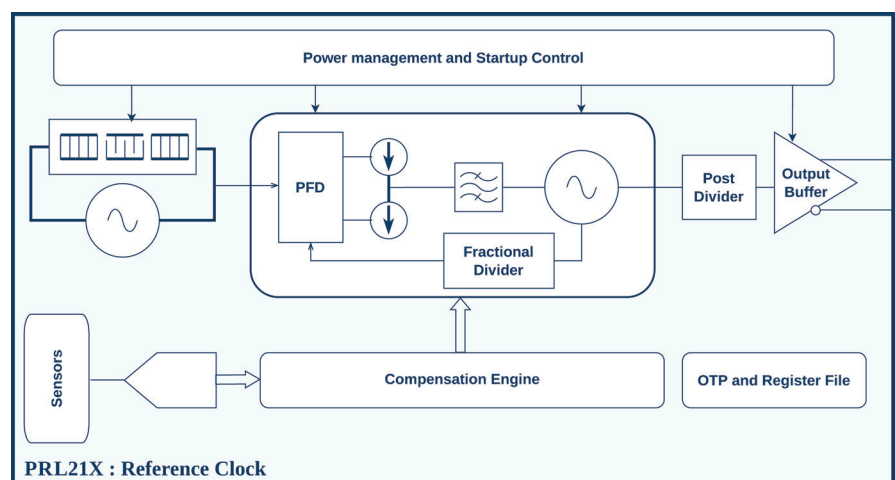
- 3.3V
- 2.5V
- 1.8V
- Auto Detect

Different O/P Formats

- CMOS (Differential & Single Ended)
- LVDS
- CML
- LVPECL
- HCSL

PRL21X is a **SingleDie™** SAW MEMS-based low noise programmable any-rate family of XOs and VCXOs. **SingleDie™** is a novel true single-die technology that has both the SAW MEMS resonator and CMOS circuitry on the same die.

Pearl utilized the **SingleDie™** technology to build **PRL21X** benefiting from the intrinsic advantages of a monolithic MEMS technology including zero thermal latency and high shock and vibration Resistance.



PRL21X supports XO, VCXO and DCXO modes, Single, Dual, Quad and Any-Rate (I2C) configurations while exhibiting low phase noise with a typical integrated RMS Jitter of 350 fs for any frequency up to 1 GHz.

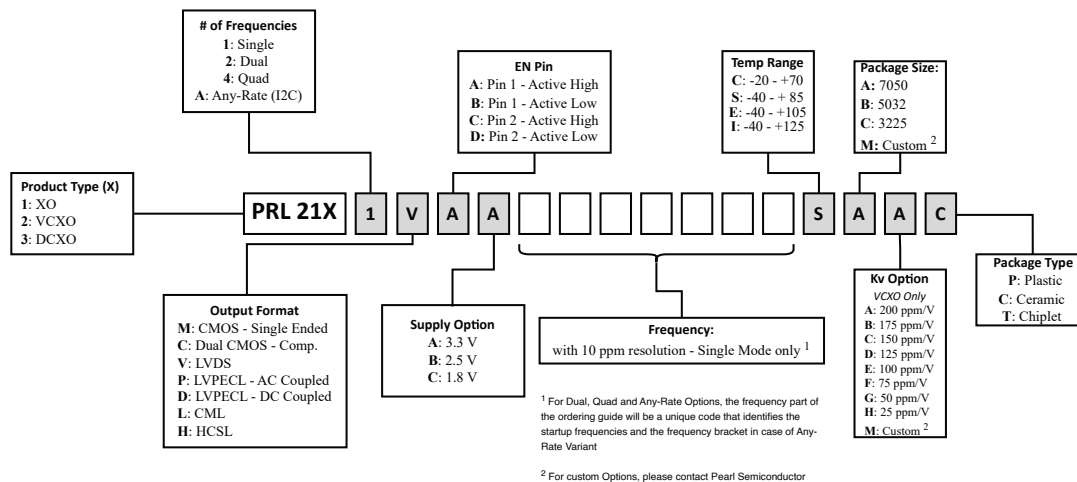
PRL21X has a novel temperature compensation engine with an integrated temperature sensor with zero thermal latency relative to the resonator. Frequency stability across an extended operating temperature range from -40 °C up to +125 °C is ±15 ppm.

PRL21X can be used in a vast range of applications including PCIe®, Networking, Industrial and Automotive applications.

PRL21X - A True Single-Die Very Low Noise XO/VCXO Family

Ordering Guide

PRL21X family comes with a vast programmability making it able to generate 100's of different part numbers. Customers can customize the part number using PRL21X ordering guide.

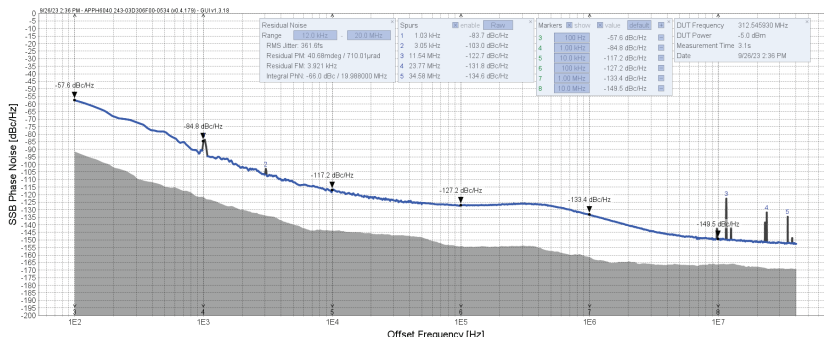


Chiplet Option

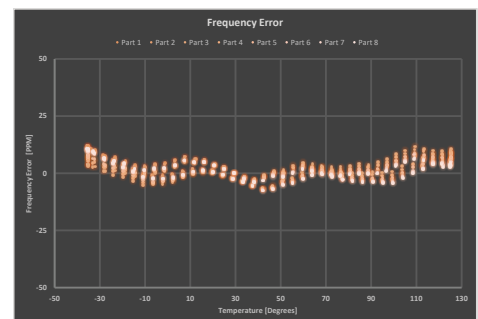
PRL21X comes also in an optional Chiplet die form with bumps that may be flip-chip soldered alongside other chiplets and devices on a substrate in a System in Package (SiP). This is a unique first in the market offering of a programmable Reference Clock chiplet integrated inside the SiP. Typically may be used in AI modules with demanding timing solutions for data computation and communication with many benefits:

- Efficient placement of the Reference Clock(s) resulting in shorter routing and higher frequency clocks and data rates.
- Saving two pins on the SiP package compared to an externally connected packaged reference clock on the board.
- Higher security level as the system clock is not accessible to be glitched or hacked disturbing any data processing or communication.
- Programmability of the clock(s) during operation allowing different modes of operation and saving power

Superior Performance



Fout = 312.5 MHz - LVDS O/P - Integrated Jitter = 361 fs



Freq Stability = ±15 ppm from -40 to +125 °C